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Engineering Note

Date: September 16,1998
Rev Date: September 16,1998

Project: CFT Axial Front End Board
Doc. No: a980916a

Subject: Analog voltage generation for SIFT control and VLPC bias

The CFT front end board contains 32 SIFT integrated circuits mounted in eight MCM modules. Each SIFT is connected via flexible circuits to 16 VLPC circuits. The VLPCs require a bias voltage in order to function that is dependent upon the operating temperature of the VLPC. Each MCM module contains four SIFT chips, and thus requires four Threshold inputs and two Range inputs.

A reasonable architecture to implement is to provide an eight-channel, eight-bit DAC for each of the eight MCM analog input areas on the CFT board. This allows modular control over the following analog parameters:

1. SIFT charge threshold, SIFT chips #1 & #2 in MCM;
2. SIFT charge threshold, SIFT chips #2 & #3 in MCM;
3. VLPC bias voltage;
4. SIFT dynamic range control voltage, chips #1 and #2 in MCM;
5. SIFT dynamic range control voltage, chips #3 and #4 in MCM;
6. SIFT VCLMP input for charge transfer control;
7. VLPC heater resistor;
8. VLPC Test Charge output.

In a normal bus environment like VME each of the 64 DAC channels would be assigned an address and directly programmed. In the CFT Axial board, the only programming access is through the 1553 bus which has a limited number of registers. A further complication is that all DAC channels must be able to be read back. A local microcontroller is present on the CFT Axial board which may be used to implement the ADC. A set of analog multiplexers is envisioned to provide the readback. To conserve 1553 register space a register with sub-addresses is proposed with the following format:

Bits	Description	Value on Read	Value on Write
15	SET_NEW/READ_CURRENT*	Always 0	If 1, causes write to DAC. If 0, causes readback via local ADC in microcontroller.
14	CONVERSION_VALID	If 1, bits 7..0 contain ADC output; if 0, bits 7..0 are invalid	No effect on write
13..11	MCM	Readback of last written value	Which MCM on the board to set or check
10..8	CHANNEL	Readback of last written value	Which DAC channel for the selected MCM to set or check
7..0	VALUE	If valid, eight-bit ADC conversion value.	Value to write to the DAC

To load a value into any DAC the system software writes a single word to the 1553 register. The 1553 interface latches the entire value and presents the appropriate write strobe dependent upon the value in bit 15 of the register. If bit 15 is set, a decoded write strobe to the selected DAC is issued. If bit 15 is a zero, a strobe to the microcontroller is issued. A block diagram of this logic is shown in Figure 1.

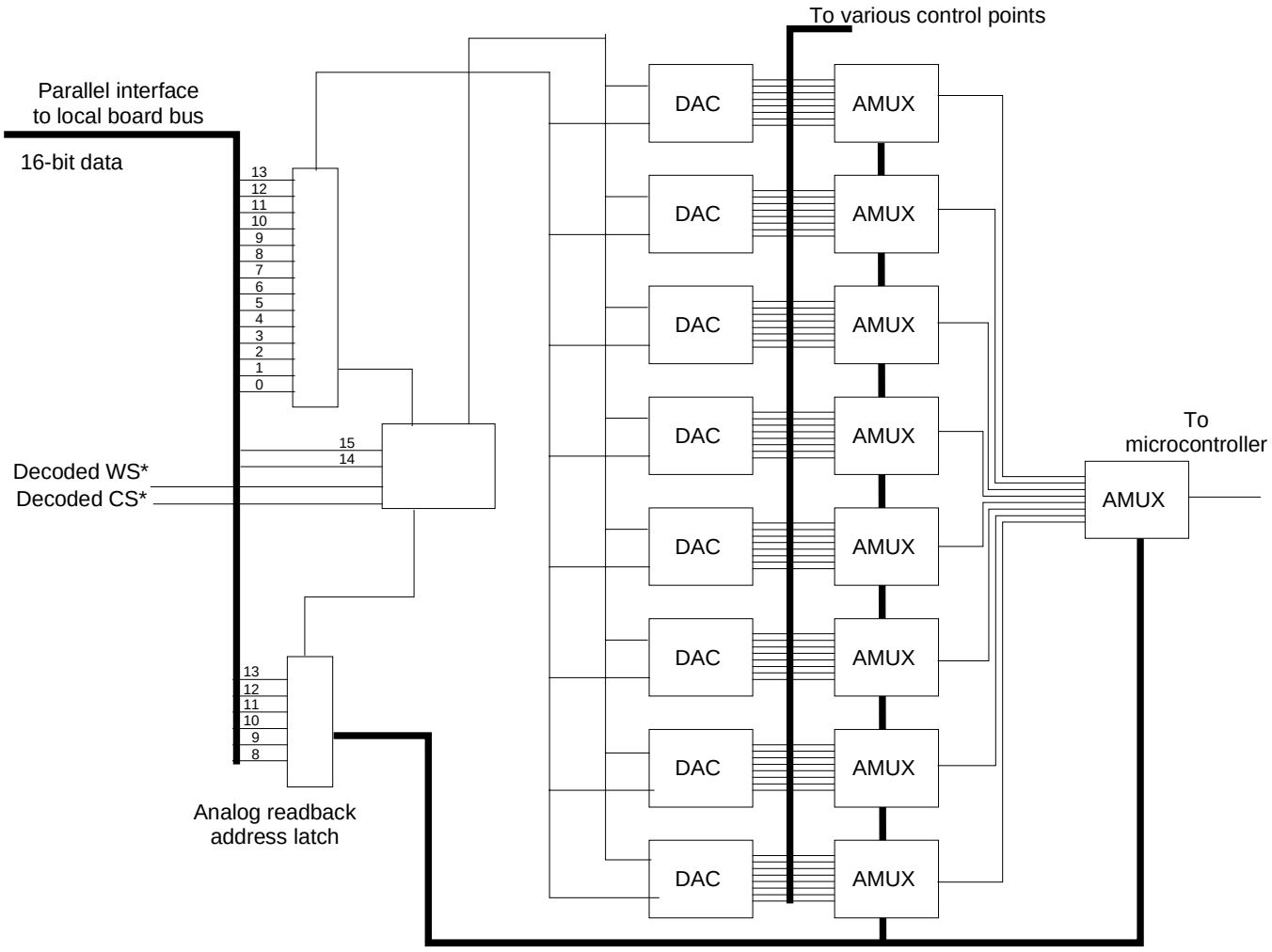

Figure 1

Detailed DAC interface

Parallel-input octal DAC components are available (e.g. Maxim MX7228) but expensive – over $30 each. With eight devices on the board, cost is a concern. Serial-input octal DACs (e.g. Maxim MX521) are available for about $4.50 each. Thus, a serial input mode is required. This places a requirement on the 1553 interface of the board that it must process DAC accesses differently than accesses to the rest of the board. Thus, as shown in Figure 1, a small interface logic piece must take the parallel data as presented to the rest of the board and re-serialize it for use with the DACs. The price of this extra logic is small – it should easily fit into a part the size of an Altera 7032 – and it saves about $200.

SIFT Threshold Control

The SIFT takes an input charge and stores it in an integrating amplifier. A reference charge is loaded into a separate capacitor which is connected to the VREF pin. The capacitor value is fixed by IC geometry at either 20 fFarad or 100 fFarad, selected by a MOSFET switch in the SIFT. Assuming that the pulse used to charge the reference capacitor is sufficiently wide to always fully charge the capacitor, the standard equation

$$Q = CV$$

applies. For a 5 volt maximum output DAC, the available maximum charge settings are then 100 fCoul or 500 fCoul. These don't match very well when compared to empirical measurements taken by F. Borcherding, copied here as Figure 2:

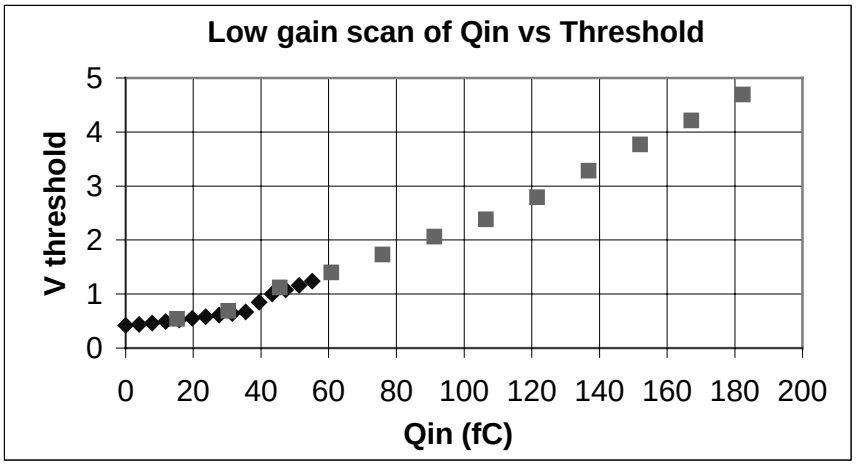

Figure 2

This graph indicates that in low gain mode, the capacitance is more on the order of 38 fFarad than the expected 100 fFarad. For this data, if a 5 volt, 8 bit DAC is used the DAC gain would be approximately .75 fCoul per count. Presumably the high gain mode still scales by a factor of five, so the expected gain in the high gain setting would be .15 fCoul per count. This is certainly far in excess of the 3 fCoul resolution discussed in earlier overviews of the board. Thus, an eight-bit DAC with a zero to five volt output range seems sufficient. In order to properly bias the SIFT, a pair of voltages is required which are centered at 2.5 volts and provide a voltage differential of from zero to five volts. Figure 3 shows a circuit which can develop this from a single DAC output.

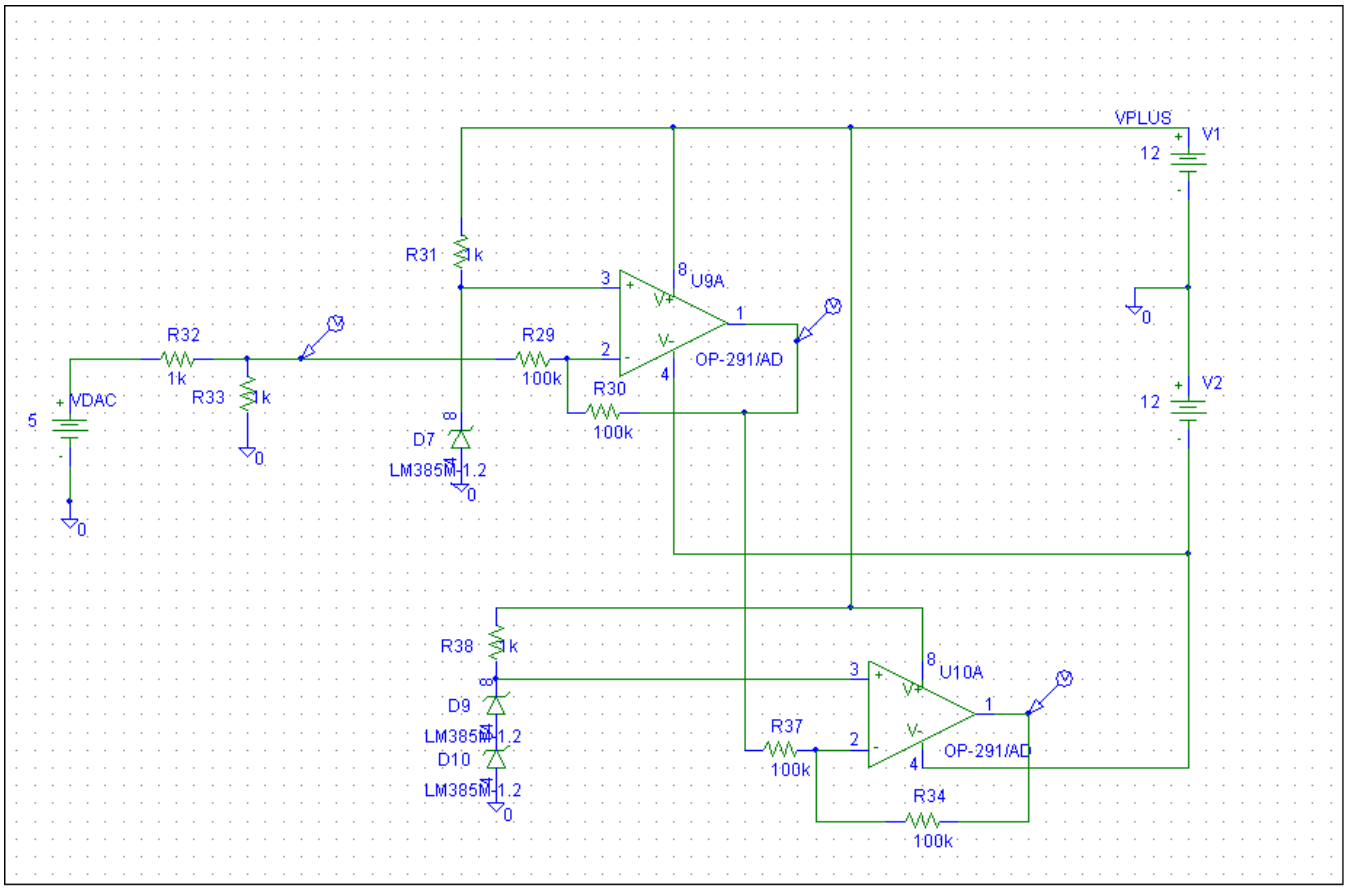

Figure 3

VLPC bias

Each VLPC cable that runs into the cryostat must supply a bias voltage to run the VLPC; this very low current voltage varies with the operating temperature from a minimum of about 6 volts to a maximum of about 10. Given that the DAC only generates a 0-5 volt output, a follower op-amp with a gain of two is required. *This also implies that the board must have an analog power supply on the order of ±12 volts.* Each of the eight VLPC bias lines also must have a current monitor. The Analog Devices AD620 is an instrumentation amplifier well suited to this task; a sketch of how this may be used is shown in Figure 4.

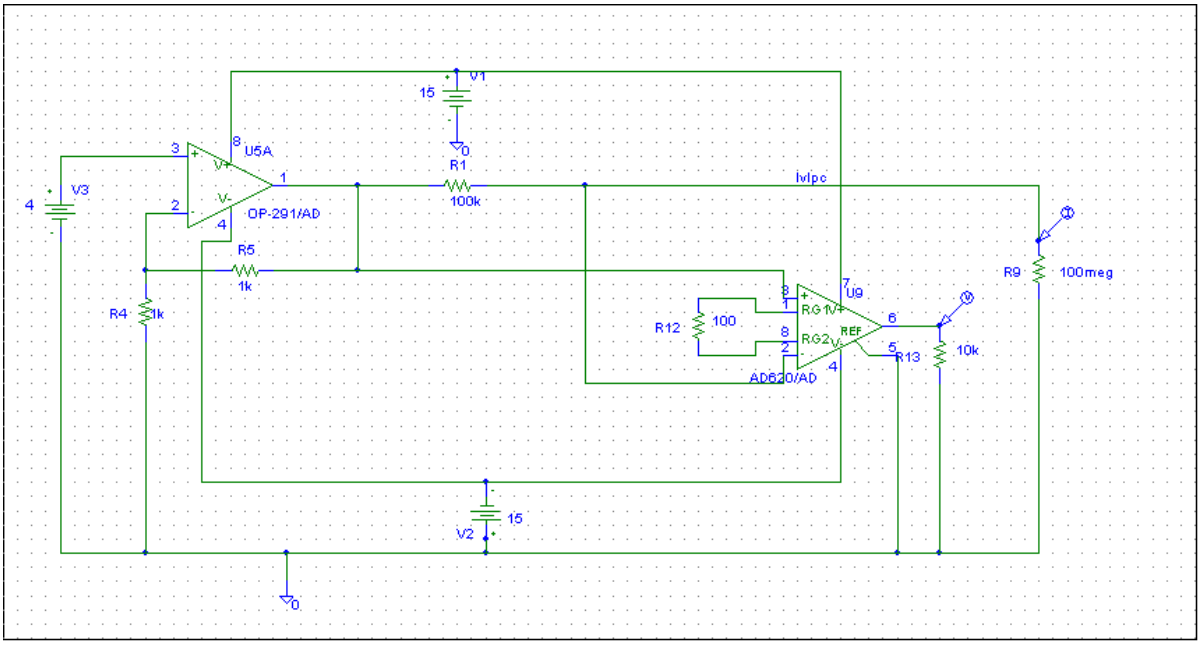

Figure 4

The 100 meg ohm resistor (R9) is a simplistic model of the VLPC. For 10 volts output it draws 100 nA. The AD620 has a bias current of a few hundred pA and so is not seriously loading the circuit. With a gain set resistor of 100 ohms and a current sensing resistor of 100 k ohms the transfer function is approximately 5 volts per 100 nA of current through the VLPC. Power supply V3 in the circuit represents the DAC output. Figure 5 shows a simulation output of the above circuit for five different temperatures (27,30,33,36,39 degrees C). The upper plot shows the output voltage to the VLPC and the output of the current monitor; the lower plot shows the current in the VLPC and the current into the monitor op-amp.

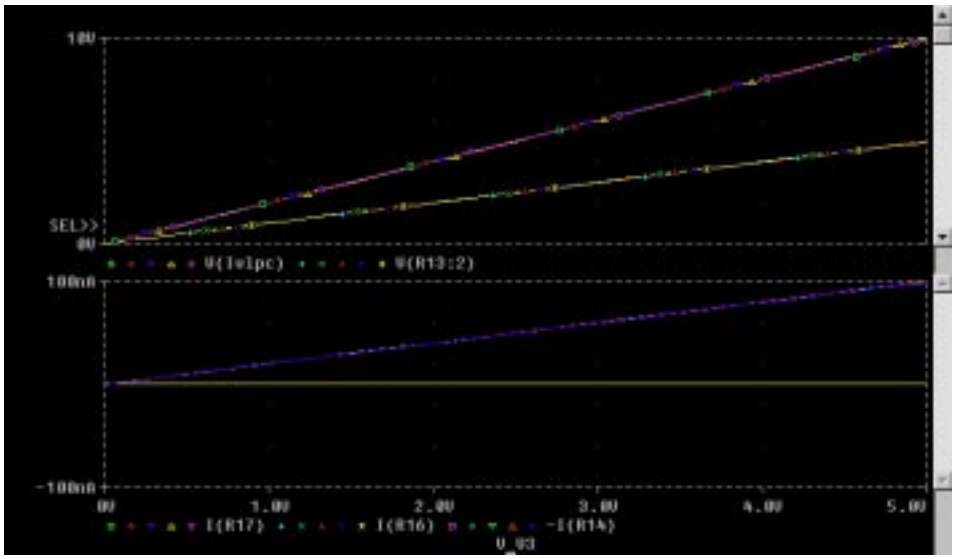

Figure 5

SIFT Dynamic Range Control Voltage

The dynamic range of the SIFT is also controlled by a voltage input. Here, a simple 0 to five volt input is provided, referenced to ground. A single channel of the DAC is wired directly to the VH_DR_A input of the MCM.

SIFT VCLMP Control Voltage

The VCLMP node of the SIFT is used to provide a reference voltage which must either source or sink current. One channel of the DAC is used, with a buffering op-amp, to maintain the node at a user-prescirbed voltage.

VLPC Heater Resistor

According to Stefan's notes, the VLPC is heated by a 500 ohm metal film resistor. Current up to 20 mA is required to provide sufficient heat. This requires that the 0-5 volt output of the DAC be buffered by an op-amp with a gain of two. The DAC channel for VLPC heat must be tied to the local microcontroller for closed loop control. This requires that the microcontroller be able to write heating values to the DAC. To accomplish this a secondary write strobe is provided in the 1553 interface which allows the microcontroller to write to any DAC channel. The microcontroller should be programmed such that it will not write values to the DAC unless enabled to do so by 1553; further, a 1553 status register should provide a bit which states whether the microcontroller is enabled to perform DAC updates or not.

To insure no collisions, 1553 updates of DAC values must first write to the microcontroller, disabling automatic temperature updates. 1553 may then write to the DACs as desired. After new values are loaded, the microcontroller is then re-enabled to write to the DACs for temperature control.